THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte KEVIN R. GRIESS,
ANN C. MERENDA and
DONALD L. PIERCE

_____

Appeal No. 97-0609
Application 08/480,106[1]

_____

ON BRIEF

_____

Before THOMAS, JERRY SMITH and FLEMING, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

[1] Application for patent filed June 7, 1995. According to the appellants, this application is a continuation of Application 08/338,976, filed November 14, 1994; which is a continuation of Application 07/807,696, filed December 16, 1991.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 14, which constitute all the claims in the application.

Representative claim 11 is reproduced below:

11. A method for dynamically handling processing errors during processing of a stream of instructions in a computer system having a plurality of functional units, comprising the steps of:

detecting an error occuring during processing of an operation subsumed by an instruction of said stream of instructions by a functional unit;

determining that said error was caused by a timing dependent defect by iteratively increasing an instruction processing cycle time and retrying at least one operation; and

after said determining step, causing said functional unit to process subsequent operations in said stream of instructions in a degraded performance mode such that said error will not recur.

The following reference is relied on by the examiner:

Missios et al. (Missios)	4,025,768	May 24, 1977

Claims 1 to 14 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Missios alone.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.[2]

OPINION

We reverse the rejection of all claims on appeal under 35 U.S.C. § 103.

Independent claims 1 and 5 on appeal here contain a common limitation relating to a feature of a means for maintaining operation of the overall computer system to continue processing of an instruction and a remainder of a stream of instructions at an instruction cycle time at which the retry of at least one earlier recited instruction was successful. Claim 5 recites essentially the same feature as in claim 1 in slightly different words.

The statement of the rejection at pages 3 and 4 of the answer does not detail the particulars of these features in each of these claims. The same may be said of the positions taken by the examiner with respect to the responsive arguments portion of the answer beginning at page 6. On the basis of this alone, it

[2] The bottom of page 1 of the principal Brief on appeal indicates that the present application is a continuation of Application Serial No. 08/338,976 filed on November 14, 1994. This latter application has been the subject of an earlier appeal identified as Appeal No. 96-1439.

appears that the examiner has not set forth a prima facie case of obviousness of the subject matter of independent claims 1 and 5 on appeal in light of the teachings and suggestions of Missios, the sole reference relied upon.

Our detailed study of this reference also leads us to conclude our agreement with appellants' basic position generally expressed at pages 14 and 15 of the principal Brief on appeal that such above noted feature set forth in both claims on appeal is not taught or suggested in the reference relied upon by the examiner. The operation of the sequence of blocks greater than block D3 in Fig. 1 of Missios does not appear to us to fuction in the manner required by the noted portion of claims 1 and 5 on appeal, since when a no error condition is obtained according to the flow diagram in Fig. 1, the sequencing of instructions does not next continue to occur at the instruction cycle time rate at which the retry was determined to be successful.

Turning lastly to the subject matter of independent claim 11 on appeal, again, we note that the statement of the rejection beginning at page 3 of the answer does not detail the particulars of this claim, the pertinent portion of which relates to the determination of an error being done by iteratively increasing an

instruction processing cycle time and then retrying at least one operation.

The responsive arguments portion of the answer beginning at the bottom of page 8 does attempt to assert the obviousness of this detailed portion of independent claim 11 on appeal. Although we understand Missios as teaching repetitively and iteratively sequencing the flow of blocks in Fig. 1 of this reference, the iterations are not done in the recited manner in independent claim 11 on appeal. Also, extending respective clock periods in a sequential or iterative manner for testing purposes is not the same as iteratively increasing an instruction processing cycle time and retrying at least one previously recited operation as set forth in claim 11 on appeal. Thus, we are in general agreement with appellants' assertion at page 15 of the principal Brief on appeal as to this claim.

In view of the foregoing, we have reversed the rejection of respective independent claims 1, 5 and 11 on appeal, necessitating in turn the reversal of their respective dependent claims. Accordingly, the decision of the examiner is reversed.

As a final matter, in view of the fact that the present application appears to be a voluntarily filed continuation of the parent application noted in footnote 2 earlier in this opinion, and since the present independent claims are variations of the subject matter of correspondingly numbered claims in that application, we further remand this application to the examiner for consideration on the record of the propriety of an obviousness-type double patenting rejection among the various claims in the two pending appeals.

REVERSED and REMANDED

JAMES D. THOMAS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)

WHITHAM CURTIS WHITHAM and MCGINN
Reston International Center
Suite 900
11800 Sunrise Valley Drive
Reston, VA 22091